REMARKS

In view of the following remarks, Applicant respectfully requests reconsideration and allowance of the subject application.

§112 Rejections

Claims 98-111 are rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. Claims 98-111 are canceled, rendering the §112 rejection moot.

§103 Rejections

Claims 98-102 and **108-111** are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over US Patent No. 5,419,712 to Bellomo et al. (hereinafter, "Bellomo") in view of US Patent No. 5,214,563 to Estes. Claims 98-102 and 108-111 are canceled, rendering the §103 rejection moot.

New Claims Allowable

New **claims 112-122** are allowable over Bellomo in view of Estes because Bellomo and Estes, alone or in combination, do not teach the elements of claims 112-122.

Applicant's independent **claim 112** recites the following:

> A chip socket assembly comprising:
>
> a chip package having a contact side, the contact side comprising a plurality of compliant contacts, the contacts adapted for detachable electrical coupling to a circuit board, the chip package having second and third sides formed with oppositely disposed protrusions;
>
> an integrated circuit disposed within the chip package, the

integrated circuit electrically coupled to the plurality of compliant contacts; and

a base formed with oppositely disposed clip portions to receive the chip package, the clip portions formed with sockets to detachably engage the chip package protrusions.

The Office asserts that Bellomo discloses a single chip package (36) configured to house a single integrated circuit chip. However, it is clear from Fig. 5 of Bellomo and its corresponding description that Bellomo does not teach a chip package at all. Rather, Bellomo teaches an edge card interconnection system that provides "enhanced electrical interconnection between ***a module and a circuit board***." (Abstract; col. 2, lines 32-34; emphasis added). "Edge card interconnection systems are known for interconnecting modules with electronic printed circuit boards. Known modules, such as single in-line memory modules (SIMM) and electronic sub-assembly daughter board modules require interconnection with a main electronic module or mother board, which typically involves implementing an edge connection scheme wherein contact pads on the edge of the module are engagable with contacts in a connector or socket on the main module or motherboard." (col. 1, lines 14-23).

Thus, Bellomo does not teach a chip package at all. It is well-known that a module such as discussed in Bellomo, is <u>not</u> the same as a "chip package" as recited in Applicant's claim 112. Rather, a module is an assembly of components (e.g., chip packages) that has some distinct function, such as a RAM module consisting of several RAM chips mounted on a small circuit board. Bellomo states that, "Known modules, such as single in-line memory modules (SIMM) and electronic sub-assembly daughter board modules require interconnection with a main electronic module or mother board, which typically involves implementing

an edge connection scheme wherein contact pads on the edge of the module are engagable with contacts in a connector or socket on the main module or motherboard." (col. 1, lines 14-23). It is well-known that a SIMM (single in-line memory module) is a module containing one or several random access memory (RAM) chips on a small circuit board with PINs that connect to a computer motherboard. Thus, it is clear that the module (36) of Bellomo is not itself a "chip package" as recited in Applicant's claim 112.

Furthermore, with respect to the teaching of a chip package, the Office sets forth inconsistent interpretations regarding Bellomo and Estes. Estes teaches thermally reactive lead assemblies and electronic circuits that contain the assemblies (col. 2, lines 55-56). In a preferred use, a plurality of leads (120) extend from a molded ceramic or plastic package (110). Estes notes that leads (120), as they are typically employed in the art, extend from the package (110) a minimum distance. Estes teaches that such lead assemblies (100) can be located well beneath the molded package (110) so as to not increase the overall printed circuit board surface area used by the electronic device. (col. 3, line 59 - col. 4, line 6). Thus, as the Office recognizes, Estes shows a chip package (110).

However, although the Office correctly interprets Estes as showing a chip package (110), it ignores the chip packages (38) of Bellomo. Instead, the Office asserts that the entire module (36) of Bellomo comprises a chip package. This assertion by the Office regarding Bellomo is not consistent with its own interpretation of Estes. Fig. 5 of Bellomo and the accompanying discussion at column 4, lines 15-30, for example, clearly indicate that Bellomo teaches a module (36) to which a plurality of chip packages (38) (e.g., memory modules)

can be connected: Bellomo states that "the module 36 includes a plurality of electronic circuits such as memory modules [chip packages] 38."

Thus, the Office interprets a chip package in one manner in Estes, while interpreting a chip package in a different manner in Bellomo. Applicant respectfully submits that a consistent interpretation of a chip package applied to both Estes and Bellomo makes it clear that Bellomo does not teach a chip package, and that Bellomo's chip module (36) is not itself, a "chip package" as recited in Applicant's claim 112.

Because Bellomo does not teach a chip package as recited in Applicant's claim 112, Bellomo cannot teach a chip package having a "contact side comprising a plurality of compliant contacts" as in claim 112. Nor can Bellomo teach that such contacts are "adapted for detachable electrical coupling to a circuit board" or that the chip package has "second and third sides formed with oppositely disposed protrusions", all of which are elements of claim 112.

Claim 112 additionally recites "an integrated circuit disposed within the chip package". Bellomo does not teach an integrated circuit disposed within a chip package. As noted above, Bellomo teaches a module (36) for connecting a plurality of chip packages (38) (e.g., memory modules). Integrated circuits are not disposed within the module (36) of Bellomo.

Claim 112 additionally recites "the integrated circuit electrically coupled to the plurality of compliant contacts". As just noted, Bellomo does not teach an integrated circuit disposed within a chip package and therefore does not teach that the integrated circuit is coupled to a plurality of compliant contacts. Bellomo does not discuss compliant contacts at all in relation to a chip package. Bellomo discusses "an edge connection scheme wherein ***contact pads on the edge of the***

module are engagable with contacts in a connector or socket on the main module or motherboard." (col. 1, lines 14-23, emphasis added). There are no compliant contacts in Bellomo to which an integrated circuit is coupled.

The Office admits that Bellomo does not teach the flexible leads (i.e., compliant contacts) of claim 112, but instead relies on Estes for such teaching. Estes teaches thermally reactive lead assemblies and electronic circuits that include a solderable, conductive metallic element having a first configuration at ambient temperature and a second expanded configuration at an elevated temperature, such as at soldering temperatures. The second configuration of the conductive metallic element provides electrical continuity between a pair of soldering locations of the electronic circuit, such as between a semiconductor device lead and a conductive surface on a printed circuit board. (Abstract).

The Office asserts at page 4 of the Office Action, that Estes teaches flexible leads 120 that are configured to provide mechanical and electrical connection between the single integrated circuit chip and the circuit board. However, Estes teaches "J" shaped leads 120 that are <u>not</u> flexible and that do <u>not</u> provide mechanical connection between the single integrated circuit chip and the circuit board.

First of all, Estes does not teach or mention that the "J" leads are flexible (compliant) as the Office asserts. The word "flexible" does not appear in Estes. Estes does not attribute flexibility or compliancy to the "J" leads. Estes does discuss deforming a coil element 50 through "cold-working" it in order to introduce residual stresses into the coil (col. 3, lines 35-45). However, even such deformation is discussed only in terms of the soldering process applied to the leads

120 and metallic elements 50. After the soldering process, there is clearly no deformation of any kind, let alone flexibility or compliancy.

Secondly, the "J" leads of Estes do not provide a mechanical connection between the single integrated circuit chip and the circuit board. Figure 5 and the related description at column 4 of Estes make clear that the "J" leads do not come into mechanical contact with the circuit board. Estes states the following:

> a plurality of lead assemblies 100 are disposed beneath each "J"-lead of the package 110, preferably after the contact surfaces on the printed circuit board 103 and the leads 120 have been sufficiently fluxed. Upon reaching soldering temperatures typically employed for reflowing operations, such as a temperature of about 320.degree.-400.degree. C., preferably about 370.degree. C., ***the solder layer 30 located on the coil-configured metallic element 50 melts to provide electrical continuity between the "J"-leads 120 and a conductive surface on the printed circuit board 103 through the metallic element 50***.
> (col. 4, lines 8-19; emphasis added).

Thus, in Estes, the metallic elements 50, and not the "J" leads, provide mechanical connection between the chip and the circuit board.

Furthermore, as noted above, Applicant's claim 112 recites "the contacts adapted for ***detachable*** electrical coupling to a circuit board" (emphasis added). From the above quotation taken from Estes, it is clear that the metallic elements 50 of Estes provide mechanical and electrical connection through a soldered connection between the "J" leads, the metallic elements 50, and the printed circuit board. A soldered connection is not detachable.

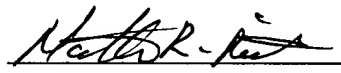
For at least the various reasons noted above, it is clear that the Bellomo and Estes references, taken alone or in combination, fail to teach the elements of Applicant's claim 112. Accordingly, claim 112 is allowable over these references.

Claims 113-122 depend directly or indirectly from claim 112, and therefore incorporate all of the elements of claim 112. Therefore, claims 113-122 are allowable by virtue of at least this dependency from claim 112 for the same reasons set forth above, and for the additional elements recited therein which are neither shown nor suggested by the cited references.

Conclusion

All pending claims are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Dated: 1/13/05 By: 

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